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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,453	MAGOSHI, HIDETAKA	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2001 and 22 April 2002 and 1*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/11/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 10 clearly recites a method for performing matrix or vector operation according to a mathematic algorithm. Claim 11 recites a computer program for performing above operations but fails to define any structural and functional interrelationships between the computer program and other claimed elements of the above operation, which permits the computer program functionality to be realized. Claim 12 recites a device for implementing the above process but fails to limit the device to any particular structure other than a general computer with input, memory, and processing devices. Indeed, any device used to implementing the underlined process would result in an apparatus as claimed. In order for such a method claim, program claim, or a device claim for implementing the underlined process to be statutory, the claim(s) must include either a step or means that results in a physical transformation outside the computer or a limitation to a practical application, at least a structural and functional interrelationships between the computer program and other claimed elements, and at least a particular structure other than general components respectively. However, it is clear from the claims that the claims merely recite step or non-specific means for data computation and

manipulation in performing a mathematical function. The input is a set of number and output is also a set of number. The claims fail to recite any step or means that results in a physical transformation outside the computer, that includes a limitation to a practical application, or that requires a structural and functional interrelationships between the computer program and other claimed elements, or that requires a specific computer to implement the claimed process. Therefore, claims 10-12 are clearly directed to a non-statutory subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazawa (J.P. 07-141325).

Re claim 1, Nakazawa discloses in Figures 1 and 5-6 a parallel arithmetic apparatus (Figure 1 wherein each of FMACs {11 & 21}, {12 & 22}, {13 & 23}, {14 & 24} processes in parallel relative to each other) comprising a plurality of pairs of recording means (e.g. 11-14) for recording arithmetical elements (e.g. Aa and Ab from 10 to each of 11-14) to be operated and operating means (e.g. 21-24) for performing sum-of-products operations (e.g. 21 sum is done by 21B and product is done by 21A) based on the arithmetical elements recorded in recording means (e.g. wherein operands of 21 are

fed from 11), wherein one of recording means of all pairs is selected (e.g. by the mux either 30a or 30b) and selecting means (e.g. 30a and 30b) for inputting arithmetical elements recorded in the selected recording means (e.g. input to mux are from 11-14) to the operating means (e.g. 21-24) of pair is inserted between the recording means and operating means pf any one pair (e.g. mux 30a is logically placed in between 11 and 21).

Re claim 2, Nakazawa further discloses in Figures 1 and 5-6 temporary recording means (e.g. a portion of 11-14 wherein the feedback from accumulators 21B-24B to 11-14 with label C) for temporarily recording mathematical elements recorded in the recording means of a pair in which selecting means is not inserted (e.g. physically the mux's 30a and 30b are not in between 12 and 22) is inserted between the recording means and operating means of pair (e.g. 11 and 21), and selecting means (e.g. 30a and 30b) is constructed in such a way as to input the arithmetical elements recorded in temporary recording means to operating means when the recording means of the pair in which selecting means is not inserted is selected (e.g. these mux are capable to input any of a or b from 11-14 into 21 as input operands).

Re claim 3, Nakazawa further discloses in Figures 1 and 5-6 recording means of all pairs record, during a matrix operation, a first arithmetical element to be subjected to matrix operation, and during a vector inner product operation, a second arithmetical element to be subjected to inner product operation (Figure 1 is capable of performing matrix and vector operations, any input element would be either matrix element or the vector element), selecting means (e.g. 30a & 30b and 51ab-54ab) is constructed, during matrix operation (e.g. 51ab-54ab takes directly from 11-14), in such a way as to input

first arithmetical element from the recording means of the own pair to the operating means of the own pair and, during inner product operation (e.g. 52ab-54ab takes directly from 12-14 and 51ab takes inputs from 30a-30b), in such a way as to select recording means of all pairs one by one in a round-robin fashion and input second arithmetical element from the selected recording means to the operating means of the own pair (e.g. 12 to 22).

Re claim 4, Nakazawa further discloses in Figures 1-2 and 5-6 each of operating means performs an operation with a content independently assigned to pair using arithmetical elements recorded in the recording means of pair (e.g. each of registers 11-14 have their own pairs of data as seen in Figure 2).

Re claim 5, Nakazawa further discloses in Figures 1 and 5-6 an operation is an operation associated with any one of four-dimensional coordinate components (Figure 6 with column as dimensions).

Re claim 6, Nakazawa discloses in Figures 1 and 5-6 a parallel arithmetic (Figure 1 wherein each of FMACs {11 & 21}, {12 & 22}, {13 & 23}, {14 & 24} processes in parallel relative to each other) apparatus that selectively performs a matrix operation (Figure 6a) and vector inner product operation (Figure 6b), comprising: a plurality of recording means (11-14) for recording, during matrix operation, a first arithmetical element (e.g. output from 10 into 11 as Ab) to be subjected to matrix operation and recording, during inner product operation, a second arithmetical element (e.g. output form 10 into 11 as Aa) to be subjected to inner product operation; a plurality of operating means (e.g. 21-24) forming a one-to-one correspondence with plurality of recording

means (e.g. 11-14) for performing during matrix operation, a sum-of-products operation (e.g. 21-24) by each operating means inputting first mathematical element recorded in the correspondent recording means, and performing during inner product operation, a sum-of-products operation by predetermined one of the operating means inputting second arithmetical element recorded in all the recording means (e.g. using mux); and selecting means (e.g. 30ab and 51ab-54ab) for selecting, during matrix operation (all mux 51ab-54ab are active), the recording means corresponding to predetermined operating means and inputting a first arithmetical element recorded in this recording means in predetermined operating means, and selecting, during inner product operation (e.g. mux 30ab active to 21), plurality of recording means one by one in a round-robin fashion and inputting a second arithmetical element recorded in the selected recording means in predetermined operating means.

Re claim 8, it is an apparatus claim of claim 6 wherein Nakazawa further discloses in Figures 1 and 5-6 the recoding means, selecting means, and operating means are registers, selector, and sum of product respectively (e.g. 11, 30a, and 21 respectively). Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 9, it is an apparatus claim of claim 8 wherein Nakazawa further discloses in Figures 2 and 6 the arithmetical elements are the coordinate values (Figures 2 and 6). Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 10, it is a method claim of claim 6. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 11, it is a computer program claim of claim 10. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 12, it is a semiconductor device claim of claim 10. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

5. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by D'Luna et al. (U.S. 5,311,459).

Re claim 10, D'Luna et al. disclose in Figures 1-3 a processing method that allows a matrix operation and vector inner product operation to be selectively executed and is executed by an apparatus provided with a plurality of operating means (general Figure 1) comprising the steps of: inputting, during matrix operation (Figure 3), arithmetical elements (C1_IN in box 12 and Coeff_IN in box 14) subjected to matrix operation by assigning the arithmetical elements to plurality of operating means (e.g. C1-C12 and I4-I6...) based on the features thereof to carry out a sum-of-products operation based on the assigned arithmetical elements (Figure 3 and col. 6 lines 37-58); and inputting, during inner product operation (Figure 2), arithmetical elements (C1_IN in box 12 and Coeff_IN in box 14) subjected to inner product operation in one predetermined operating means to allow operating means to carry out a sum-of-products operation based on the arithmetical elements (Figure 2 and col. 4 lines 45-62).

Re claim 11, it is a computer program claim of claim 10. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 12, it is a semiconductor device claim of claim 10. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being obvious over Nakazawa (J.P. 07-141325).

Re claim 7, Nakazawa further discloses in Figures 1 and 5-6 an arithmetical element is expressed with a number and operating means is constructed so as to perform a sum-of-products operation of the number (e.g. 21 with multiplication 21A and accumulation 21B). Nakazawa does not disclose the number is floating-point. However, the examiner takes an official notice that MAC operation in floating-point is well known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the number as floating-point as well known into Nakazawa's invention because it would enable to simplify and improve accuracy of system in many applications.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,557,022 to Sih et al. disclose a digital signal processor with coupled multiply-accumulate units.

b. U.S. Patent No. 6,138,136 to Bauer et al. disclose a signal processor.

c. U.S. Patent No. 6,606,700 to Sih et al. disclose a DSP with dual-MAC processor and dual-MAC coprocessor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

January 5, 2005

TODD INGBERG
PRIMARY EXAMINER